IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Patent Application No. 10/541,275

Confirmation No. 6275

Applicant: Moreira et al.

Filed: June 30, 2005

TC/AU: 2183

Examiner: Vicary, Keith E.

Docket No.: 260686

Customer No.: 23460

APPELLANTS' APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In support of the appeal from the final rejection dated March 30, 2009, Appellants now submit their Brief.

Real Party In Interest

The patent application that is the subject of this appeal is assigned to Koninklijke Philips Electronics N.V.

Related Appeals and Interferences

There are no appeals or interferences that are related to this appeal.

Status of Claims

Claims 1-6, 8-14 and 16-29 are presently pending.

Claims 7 and 15 were canceled.

Claims 1-6, 8-14 and 16-29 stand finally rejected, and these rejections are presently being appealed.

A complete listing of claims 1-6, 8-14 and 16-29 appears in the Claims Appendix.

Status of Amendments

An amendment was submitted after the Final Office Action from which the present appeal was taken. The claim amendments, addressing each of the Section 112, paragraph 2 rejections, have been entered, and the Advisory Action dated September 9, 2010, withdraws all previous Section 112 rejections (see, pages 2-3 of the Final Office Action). The Claims Appendix thus incorporates the amendments after the Final Office Action.

Summary of Claimed Subject Matter

Claims 1-6, 8-14 and 16-29, including independent claims 1 and 29, are pending. The summaries of the claims reference the specification and drawings filed with the PCT application PCT/IB2003/005926 (International Publication Number WO 2004/059464) to which this application, filed on June 30, 2005, claims priority.

Independent **claim 1** is directed to a processing system comprising a plurality of processing elements. *See, e.g,,* FIG. 5 and specification, page 6, line 33, to page 7, line 20. The processing elements (PE_j and PE_{j+1}) comprise a controller (CT) and computation means (ALU). See, FIG. 2, page 4, lines 23, et seq.

The plurality of processing elements (PE) are dynamically reconfigurable by a cluster control signal (*see*, input C in each PE in FIGs. 3 and 5, page 5, lines 20-30) as either:

(1) mutually independently operating task units that comprise one processing element (PE); or

(2) a cluster of two or more processing elements where the processing elements within a cluster are arranged to execute instructions under a common thread of program control. *See*, FIGs. 3 and 5, page 1, line 27 to page 2, line 6, and page 5, lines 20-30.

The cluster control signal (C) for a processing element (PE) is derived from intermediate control signals (e.g., L1 and L2). (see, FIGs. 5 and 6, L1 and L2) transmitted through a reconfigurable channel infrastructure (see, FIG. 3, CH) connected to the processing elements (PE). See, FIGs 3, 5 and 6, page 5, lines 18-20 and page 7, lines 1-20.

Moreover, the reconfigurable channel (CH) infrastructure comprises a control chain (*see*, FIGs. 5 and 6, "CHN" element, and page 7, lines 1 et seq.) including:

(1) combination elements (*see, e.g.,* FIG. 5, $c_{j,1}$, $c_{j,2}$, $c_{j+1,1}$, and $c_{j+1,2}$) for each processing element (PE), and

(2) a programmable switch (*see, e.g.*, FIG. 5, $SW_{j,j+1}$) between each pair of neighboring processing elements (*see, e.g.*, PE_j and PE_{j+1}) for locally controllably inhibiting transmission of intermediate control signals (L1' and L2) to a preceding or a succeeding processing element (PE_j and PE_{j+1}). *See,* FIG. 5, page 7, lines 1-13.

Dependent **claim 2** is directed to the processing system according to claim 1, wherein processing elements organized in a task unit share the cluster control signal for controlling instruction execution. See, FIG. 3, page 5, line 18 to page 6, line 5.

Dependent **claim 6** is directed to the processing system according to claim 5, wherein the data-path connections are limited to neighbor-to-neighbor connections. See, FIG. 1, page 4, lines 13-19.

Dependent **claim 12** is directed to the processing system according to claim 1, wherein the reconfigurable channel infrastructure comprises mutually transverse chains. *See*, FIG. 7, page 8, lines 11-18.

Independent **claim 29** is directed to a method for operating a processing system comprising a plurality of processing elements (see, FIG. 5, PE_j and PE_{j+1}). The processing elements (PE_j and PE_{j+1}) comprise a controller (FIG. 2, CT) and computation means (e.g., FIG. 2, ALU). The method comprising the steps of:

(a) combining, by a combination element (*see, e.g.,* FIG. 5, $c_{j,1}$), an intermediate control signal (L1) with an operation control signal (F_j) of a processing element (PE_j), and selectively passing ($SW_{j,j+1}$) the combined signal (L1') to a further processing element (PE_{j+1}). See, FIG. 5, page 7, lines 1-13.

(b) deriving a cluster control signal (*see, e.g.,*, FIG. 5, input C in PE_j) from an operation control signal (F_j) and two or more intermediate control signals (L1, L2). *See, Id.*

(c) dynamically reconfiguring a processing element by the cluster control signal (*see, e.g,* input C of PE_j) thereby dynamically reconfiguring the plurality of processing elements (*see,* FIG. 5, PE_j and PE_{j+1}) as mutually independently operating task units that comprise either:

(1) one processing element, or

(2) a cluster of two or more processing elements, wherein the processing elements within a cluster execute instructions under a common thread of program control. *See*, FIGs. 3 and 5, and page 1, line 27 to page 2, line 6; page 5, lines 20-30; and page 7, lines 13-20.

Grounds of Rejection to be reviewed on Appeal

The grounds of rejection to be reviewed on appeal are the grounds stated in the Final Office Action mailed on March 30, 2009. In particular, Appellants appeal the rejection of:

1. Claims 1-6, 8, 12-14, 18-22, and 28-29 under 35 U.S.C. §102(b) as being anticipated by Gove et al., US Pat. No. 5,212,777 (hereinafter "Gove").

2. Claims 9-11 and 16-17 under 35 U.S.C. §103(a) as being unpatentable over Gove in view of Belton's *Basic Gate and Functions* website (hereinafter "Belton").

3. Claim 23 under 35 U.S.C. §103(a) as being unpatentable over Gove.

4. Claims 24-27 under 35 U.S.C. §103(a) as being unpatentable over Gove in view of Pechanek et al., US Pat. No. 6,151,668 (Pechanek).

5. Claims 6 and 28 under 35 U.S.C. 103(a) as being unpatentable over Gove in view of Parcerisa et al.'s *Efficient Interconnects for Clustered Microarchitectures* publication (hereinafter "Parcerisa").

Argument

Appellants request reversal of the Final Office Action's rejection of the presently pending claims 1-6, 8-14 and 16-29 in view of Appellants' remarks provided herein. In summary, the Final Office Action's rejection of the presently pending claims is based upon a claim construction that expands the breadth of recited claim elements beyond reasonable claim scope boundaries inasmuch as the scope of claim elements asserted in the Final Office Action is inconsistent with (1) Appellants' disclosure, (2) previous amendments and (3) Appellants' remarks, in previous Office Action responses, explaining the scope of the presently appealed claims. Appellants address the particular grounds for rejection herein below.

For the reasons presented herein Appellants request reversal of the Final Office Action's rejection of each of the presently pending claims (1-6, 8-14 and 16-29).

1. Rejection of Claims 1-6, 8, 12-14, 18-22, and 28-29 as anticipated by Gove

Claims 1, 3-5, 8, 18-22, and 28

The claimed invention

The presently appealed claim 1 directed to a processing system including a set of processing elements that are configurable into sub-sets (clusters) of processing elements (PEs) that operate under a common thread of program control. The clusters are established using a reconfigurable channel infrastructure comprising a *control chain* (see, FIG. 5, CHN). The control chain includes a **programmable switch** (SW's controlled by control signals "E") **between neighboring processing elements** (PEs) **to locally controllably inhibit transmitting intermediate control signals** (L1, L2, L1', and L2') **to neighboring (preceding/succeeding) processing elements**. A detailed summary of Appellants' invention is provided herein above.

Gove

In contrast to Appellants' claimed *control chain* within a reconfigurable channel infrastructure, Gove (see, FIG. 22) discloses a cluster *control bus* structure that supplies cluster selection signals via a SYNC'D signal bus 40. Activation of particular processing elements is achieved via direct control lines (transmitting EXECUTE signals) from a set of independent programmable SYNC control elements to corresponding individual processing elements.

Gove's SYNC control elements are initially programmed by storing a cluster ID in a "sync control register." Thereafter, the system activates a set of clustered processing elements by providing the appropriate cluster ID (e.g., 1001 or 0110) via SYNC'D signals transmitted on bus lines 40. The SYNC'D value transmitted on bus lines 40 are compared to cluster ID values stored in the SYNC CONTROL registers for each of the (four) individual processing elements. If the value on the lines 40 matches the pre-stored cluster ID for a given SYNC control element, then the "EXECUTE" signal is activated for a particular processing element associated with the SYNC control having a matching cluster ID.

FIG. 22 of Gove unequivocally discloses a set of SYNC controls that activate corresponding individual processing elements (via output EXECUTE signals) when the input SYNC'D signal values provided by the bus 40 match a designated cluster ID stored in a SYNC control register. The SYNC'D signals are provided *directly from SYNC'D bus 40* to each of the SYNC controls (four such independently controlled circuits being shown in FIG. 22).

Importantly, the Final Office Action, at page 5, lines 4-6, states that the recited "intermediate control signals" are the SYNC'D signals carried by bus 40. **However, FIG. 22 of Gove does not disclose any "programmable switch between each pair of neighboring processing elements" that inhibits transmitting the SYNC'D signals to a preceding/succeeding processing element. In fact the SYNC'D signals (received by the SYNC control circuits) aren't even transmitted to a processing element.** Gove does not disclose Appellants' claimed "programmable switch between each pair of neighboring processing elements for controllably inhibiting transmission of *intermediate control signals* to a preceding or a succeeding processing element." (emphasis added). Since Gove does not disclose the recited "programmable switch" and its associated functionality regarding transmitting the intermediate control signals to neighboring processing elements, Gove does not anticipate claim 1.

Gove does not anticipate the claimed invention

The Final Office Action repeatedly emphasizes that the recited claims can be interpreted very broadly to encompass the processor cluster control circuit disclosed in FIG. 22 of Gove. Appellants object to a current interpretation, by the Final Office Action, of the appealed claims that skews, among other things, the meaning of the recited "control chain" and "programmable switch" elements that have been defined by Appellants' disclosed embodiments. Appellants

submit that during prosecution of an application, claims must be given a broadest *reasonable* interpretation. See, *Phillips v. AWH Corp.*, 75 USPQ2d 1321 (Fed. Cir. 2005). This decision of the Federal Circuit applies to both application prosecution and patent litigation contexts. As explained in *Phillips*, claims must be reasonably interpreted *in view of the specification*, which is highly relevant to claim construction analysis, and is the *single best guide to determining the meaning of terms*.

An application's specification and drawings must be considered when determining a reasonable scope of recited elements of a claimed invention. However, the Final Office Action (dated March 30, 2009) and the Advisory Action (dated September 9, 2009) disregard Appellants' description of the invention in the specification and drawings (see, FIG. 5) when construing the recited elements of the claimed "reconfigurable channel infrastructure" comprising a "control chain" (see, FIG. 5, CHN). The Final Office Action rejects independent claim 1 based upon an unreasonable interpretation of the aforementioned claim element. The portions of claim 1 defining the relationships between the recited sub-elements of the "reconfigurable channel infrastructure" as well as their overall function (i.e., controllably inhibiting transmission of intermediate control signals to a preceding or a succeeding processing element) are improperly disregarded.

FIG. 22 of Gove, and the associated written description, neither discloses nor suggests Appellants' claimed *control chain* (CHN) containing a *programmable switch* (SW) between each processing element for "locally controllably inhibiting transmission of intermediate control signals" to neighboring processing elements. It is the programmable switches between neighboring processing elements that creates the recited control *chain* structure – as opposed to the control *bus* structure disclosed in FIG. 22 of Gove. Instead of interposed programmable switches (resulting in the claimed control chain), *each processing element* in Gove is provided an independently rendered activation control signal (i.e., EXECUTE signal rendered by a SYNC control for the particular processing element). Each EXECUTE signal is independently rendered with respect to each of the other EXECUTE signals in the set of four cluster control elements depicted in FIG. 22 of Gove. Moreover, each SYNC control circuit independently receives cluster ID information via bus 40's SYNC'D signals. There is thus no "chain" aspect of the control architecture disclosed in Gove's FIG. 22.

The Final Office Action asserts, at page 5, lines 4-6, that the recited "intermediate control signals" correspond to Gove's SYNC'D signals (on bus 40 in FIG. 22). Moreover, the Final Office Action, at page 5, lines 10-14, states that the claimed "programmable switch" is any of the NAND gates in FIG. 22. However, Gove does not disclose any NAND gates (i.e., "programmable switches") that are located *between each pair of neighboring processing elements* and that controllably inhibit transmission of the SYNC'D signals (i.e., "intermediate control signals") to a preceding or a succeeding processing element. The NAND gates depicted in FIG. 22 are not positioned *between neighboring processing elements* (not shown in FIG. 22) in any way that the NAND gates could locally controllably *inhibit transmission of the SYNC'D signals (on bus 40) to a preceding/succeeding processing element* in accordance with claim 1. **In fact, the SYNC'D signals are merely address signals that *terminate at the logic inputs of the NAND gates* in FIG. 22 of Gove. Nowhere does Gove disclose that the SYNC'D signals are somehow controllably inhibited from passing from one processing element to a proceeding/succeeding processing element as recited in the final clause of claim 1.**

In summary, Gove implements multiprocessor cluster control in a way that substantially differs from the recited cluster control hardware recited in claim 1. Gove discloses a *control bus* for delivering a set of address signals in parallel to a full set of cluster (sync) controllers for individual processing elements. Nowhere does Gove disclose or even remotely suggest Applicants' recited *control chain* structure including a set of programmable switches implementing localized serial cluster control of a set of processing elements. While both Gove and Applicants' disclosed/claimed cluster control hardware facilitate flexibly clustering processing elements, Gove achieves clustering via an address bus wherein each SYNC controller for a corresponding processing element is provided with individual direct connections to a universal set of cluster control (cluster ID) signal lines. In contrast, Applicants' claimed reconfigurable channel infrastructure includes a *control chain* for passing cluster signals to the processing elements via programmable switches capable, at each link between two processing elements, of locally inhibiting transmission of intermediate cluster control signals to neighboring processing elements.

For the above reasons, Gove does not disclose Appellants' claimed "programmable switch between each pair of neighboring processing elements for controllably inhibiting transmission of *intermediate control signals* to a preceding or a succeeding processing element."

(emphasis added). Therefore, the anticipation rejection of claim 1 based on Gove should be withdrawn/reversed.

In the event the rejection of claim 1 is not reversed/withdrawn Appellants specifically request identification of any structure in Gove's bus-based multiprocessor cluster control that corresponds to Appellants' claimed "control chain" (as opposed to Gove's control bus 40) including a "programmable switch" that controllably inhibits transmission of the intermediate control signals (i.e., the SYNC'D signals on bus 40 according to the Final Office Action) between a processing element and its neighboring processing elements.

Claim 2

Appellants request reversal of the rejection of **claim 2** because Gove does not disclose that processing elements organized in a task unit share the cluster control signal for controlling instruction execution. By virtue of the "OR" logic and switches that selectively connect the operational control signal for a configured cluster of processing elements, the disclosed processing system enables sharing the cluster control signal between each processing element within a cluster. The SYNC'D signals, to which the Final Office Action refers, are not even the cluster control signal. Instead the SYNC'D signals, *previously identified by the Final Office Action as the intermediate control signals,* provide an ID to *select* a set of synchronized processors engaged in a *same* task. The resulting EXECUTE signals are independently rendered and provided on a one-to-one basis by the SYNC controllers to their respective processing element. See, FIG. 22 EXECUTE signals rendered by SYNC Controllers 0-3. Therefore, when Gove's invention is in SIMD mode, the processing elements fetch from the same instruction memory under *separate* (though synchronized) control signals (see, e.g., each separately provided EXECUTE signal by the SYNC controllers in FIG. 22).

Claim 6

Appellants request reversal of the rejection of **claim 6** since Gove does not disclose that data-path connections (DPC) are *limited* to neighbor-to-neighbor connections. To the extent that Gove's SYNC'D signals on bus 40 are considered DPC's, such signals are provided to *every* SYNC controller. Thus the recited "limited to neighbor-to-neighbor connections" is not disclosed in Gove.

Claims 12-14

Appellants request reversal of the rejection of **claim 12** (and dependent claims 13 and 14) since Gove does not disclose a "channel infrastructure [comprising] mutually transverse chains." As defined by Appellants' specification and drawings, "transverse chains" correspond to the vertical and horizontal control chains that, aside from their path orientation, are otherwise equivalent. The Final Office Action identifies an alleged horizontal chain corresponding to a bus 40 carrying the SYNC'D signals to all SYNC controllers (for corresponding processing elements). The vertical lines and associated circuits (i.e., NAND gates and sync control registers) drawn from the horizontal SYNC'D bus 40 lines cannot correspond to transverse chains since there is no identifiable series of consecutive identical elements.

Claim 29

Appellants traverse the anticipation rejection of claim 29 since Gove does not disclose each of the steps of the recited method. Claim 29 recites a step of combining, by a combination element (*see, e.g.,* FIG. 5, $c_{j,1}$), an intermediate control signal (e.g., L1) with an operation control signal (F_j) of a processing element (PE_j) and selectively passing (see, e.g,, $SW_{j,j+1}$) the combined signal (L1') to a further processing element (PE_{j+1}). See, FIG. 5, page 7, lines 1-13.

Gove neither discloses nor suggests the recited step of "combining" an intermediate control signal with an operation control signal of *a processing element* to render a combined signal that is thereafter sent to another processing element. As noted above, Gove discloses placing a cluster ID on SYNC'D signals of bus 40 to select a particular processing element cluster. The Final Office Action identifies the SYNC'D signals as corresponding to the recited intermediate control signal. Gove unequivocally discloses independent activation of individual SYNC Control elements through dedicated logic (SYNC Control) circuits. Nowhere does Gove even remotely suggest that an operation control signal (F_j) *from a processing element* is combined with the SYNC'D signal transmitted via bus 40 and selectively passed (e.g, via switch SW) to yet another processing element. **In the event that the rejection of claim 29 is not withdrawn, Appellants request specific identification of: (1) the operation control signal from a processing element, (2) the "combination element" that combines the "operation control signal of a processing element" with the SYNCH'D signal, and (3) the resulting combined signal that is *selectively passed* to**

another processing element – noting that the combined signal cannot be the EXECUTE signal which, according to the Final Office Action, is the "cluster control signal".

As noted previously above with regard to the rejection of claim 1, Gove discloses a *control bus* (SYNC'D bus 40) that carries a set of cluster ID signals in parallel to each SYNC controller associated with a corresponding processing element. Therefore, Gove does not disclose "selectively passing" the recited "combined signal" to a further processing element.

2. Rejection of Claims 9-11 and 16-17 as obvious over Gove in view of Belton

Appellants have not separately argued the obviousness rejections of claims 9-11 and 16-17 over Gove in view of Belton. However, such claims are at least patentable for the reasons set forth herein above regarding independent claim 1 from which each depends.

3. Rejection of Claim 23 as obvious over Gove

Appellants have not separately argued the obviousness rejections of claim 23 over Gove. However, claim 23 is at least patentable for the reasons set forth herein above regarding independent claim 1 from which claim 23 depends.

4. Rejection of Claims 24-27 as obvious over Gove in view of Pechanek

Appellants have not separately argued the obviousness rejections of claims 24-27 over Gove in view of Pechanek. However, such claims are at least patentable for the reasons set forth herein above regarding independent claim 1 from which each depends.

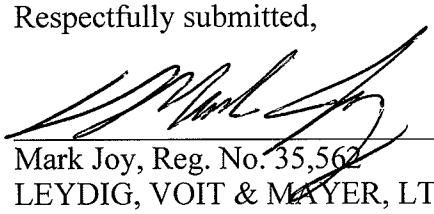
5. Rejection of Claims 6 and 28 as obvious over Gove in view of Parcerisa

Appellants traverse the obviousness rejection of **claim 6** over Gove in view of Parcerisa. While Parcerisa may indeed espouse the virtues of neighbor-to-neighbor connections, there is absolutely no reasonable basis for one skilled in the art to modify the SYNC'D bus 40 such that it comprises a set of neighbor-to-neighbor data connections. The lines carrying the cluster ID on the SYNC'D bus 40 must be provided *in all instances* to *each SYNC controller*. Under such circumstances there is no logical reason to substitute the universal bus structure for a series of neighbor-to-neighbor connections (and the resulting delay in passing the necessary cluster ID value to each processing element). For at least this further reason, claim 6 is not rendered obvious by the combined teachings of Gove and Parcerisa.

Conclusion

The presently claimed invention would not have been anticipated or rendered obvious to one having ordinary skill in the art at the time of the invention. Each of the presently pending claims is patentable over the prior art presently known to Appellants for at least the reasons set forth herein. Appellants therefore request reversal of the presently pending rejection of claims 1-6, 8-14 and 16-29.

Respectfully submitted,



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Claims Appendix

1. (Previously presented) A processing system comprising a plurality of processing elements, the processing elements comprising a controller and computation means, the plurality of processing elements being dynamically reconfigurable by a cluster control signal as mutually independently operating task units that comprise one processing element or a cluster of two or more processing elements, the processing elements within a cluster being arranged to execute instructions under a common thread of program control, wherein the cluster control signal is derived from intermediate control signals transmitted through a reconfigurable channel infrastructure connected to the processing elements, wherein the reconfigurable channel infrastructure comprises a control chain with combination elements for each processing element and a programmable switch between each pair of neighboring processing elements for locally controllably inhibiting transmission of intermediate control signals to a preceding or a succeeding processing element.

2. (Previously presented) Processing system according to claim 1, wherein processing elements organized in a task unit share the cluster control signal for controlling instruction execution.

3. (Previously presented) Processing system according to claim 2, wherein the cluster control signal is a flag controlling a guarded operation.

4. (Original) Processing system according to claim 3, wherein the guarded operation is a conditional jump.

5. (Previously presented) Processing system according to claim 1, wherein the processing elements are connected to each other via data-path connections.

6. (Previously presented) Processing system according to claim 5, wherein the data-path connections are limited to neighbor-to-neighbor connections.

7. (Canceled).

8. (Previously presented) Processing system according to claim 1, wherein the cluster control signal is derived by combining the intermediate control signals through a combination element associated with each processing element.

9. (Previously presented) Processing system according to claim 8, wherein the combination element associated with each processing element consists of an OR-gate.

10. (Previously presented) Processing system according to claim 1, wherein the reconfigurable channel infrastructure comprises programmable sum-terms.

11. (Previously presented) Processing system according to claim 1, wherein the reconfigurable channel infrastructure comprises programmable product-terms.

12. (Previously presented) Processing system according to claim 1, wherein the reconfigurable channel infrastructure comprises mutually transverse chains.

13. (Previously presented) Processing system according to claim 12, wherein the combination elements are arranged in chains having a first orientation and chains having a second orientation, and wherein the intermediate control signals transmitted through the chains having the first orientation are forwarded to the combination elements in the chains having the second orientation.

14. (Original) Processing system according to claims 13, wherein the intermediate control signals transmitted through the chains having the second orientation are forwarded to the combination elements in the chains having the first orientation.

15. (Canceled).

16. (Previously presented) Processing system according to claim 1, wherein the combination elements consist of OR-gates.

17. (Previously presented) Processing system according to claim 1, wherein the programmable switch between neighboring processing elements comprises AND-gates.

18. (Previously presented) Processing system according to claims 1, wherein the programmable switch between neighboring processing elements is programmed by a signal stored in a memory cell.

19. (Previously presented) Processing system according to claim 18, wherein at least one of the processing elements can write to at least one memory cell.

20. (Previously presented) Processing system according to claim 18, wherein a set of memory cells used to program a set of the programmable switches between neighboring processing elements is organized as a data-word in a memory.

21. (Previously presented) Processing system according to claim 20, wherein the memory contains multiple data-words, and wherein the programmable switches are programmed by selecting one of the data-words.

22. (Original) Processing system according to claims 21, wherein one or more of the processing elements can program the programmable switches by dynamically selecting the data-word in memory.

23. (Previously presented) Processing system according to claims 18, wherein the memory consists of volatile random access memory.

24. (Previously presented) Processing system according to claim 1, wherein each single processing element is capable of executing a VLIW instruction.

25. (Previously presented) Processing system according to claim 24, wherein the processing element comprises an internal interconnect network.

26. (Previously presented) Processing system according to claim 25, wherein the internal interconnect network consists of point-to-point connections.

27. (Previously presented) Processing system according to claim 25, wherein the internal interconnect network comprises data-path connections to a set of operation issue slots within the processing elements.

28. (Original) Processing system according to claim 1, wherein the processing elements are arranged in a 2-dimensional grid.

29. (Previously presented) Method for operating a processing system comprising a plurality of processing elements, the processing elements comprising a controller and computation means, the method comprising the steps of:

combining, by a combination element, an intermediate control signal with an operation control signal of a processing element and selectively passing the combined signal to a further processing element,

deriving a cluster control signal from an operation control signal and two or more intermediate control signals, and

dynamically reconfiguring a processing element by the cluster control signal thereby dynamically reconfiguring the plurality of processing elements as mutually independently operating task units that comprise one processing element or a cluster of two or more processing elements, wherein the processing elements within a cluster execute instructions under a common thread of program control.

Evidence Appendix

NOT APPLICABLE

Related Proceedings Appendix
NOT APPLICABLE